REMARKS

The Examiner's Action mailed on December 1, 2004 has been received and its contents carefully considered. Claims 3, 10, 12 and 28, have been amended, and a new claim 29 has been added to further protect the invention. Reexamination and reconsideration of the amended application respectfully is requested. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner rejected claims 3, 4 and 6 under 35 USC 112, first paragraph, on grounds that the specification is silent as to bracing and a mechanism for inhibiting warpage recited in claim 3, and claims 4 and 6 depend from claim 3. Claim 3 has been amended to change the claim language at issue to specify with respect to the bracing step, only that bracing the substrate with the back side resin layer is preformed until after the surface grinding step. Support in the specification for the presence of the back side resin layer during the surface grinding step is not at issue and the bracing function is deemed clearly to be inherent by its presence to inhibit warpage until the grinding of that back side resin layer. The rejection accordingly should be withdrawn.

The Examiner also rejected claims 26-28 under 35 USC 112, first paragraph, on grounds that the specification does not support recitations therein, namely that the specification does not support: (1) surface grinding such that the remaining surface layer has a thickness that is uniform at least within the cutting lines defining the individual pieces cut out of semiconductor devices in the cutting out step (claim 26); (2) forming a surface resin layer to include forming the surface layer with uniform thickness (claim 27); or (3) surface grinding step to include

grinding the surface resin layer so that the heights of the plurality of projection electrodes is uniform. The rejection respectfully is traversed. The limitations of which the Examiner speaks are supported in the specification respectively at page 29, page 27 and page 27, and all are supported in the drawings. The rejections accordingly should be withdrawn.

The Examiner also rejected claims 10, 12 and 17-21 under 35 USC 103(a) as being unpatentable over *Sekine et al.* in view of *Admission* or *Frye et al.* The rejection of claims 17-21 respectfully is traversed. Claim 10 has been amended, and it is submitted that the rejection is inapplicable to the amended claims.

Claim 10 has been amended further to clarify that the structure defined in the claim is on a wafer level basis so that a plurality of separate chip-on-chip devices can be produced therefrom. That is, claim 10 has been amended to clarify that the semiconductor device of the invention includes a solid device including an undivided semiconductor wafer having formed therein a plurality of semiconductor chip elements, that the chip elements respectively are disposed below the semiconductor chips bonded on the solid device, such that the semiconductor chips and the respective semiconductor chip elements are separable as units into separate respective chip-on-chip structures, by a procedure that includes cutting the wafer along cut lines thereof.

The references alone or in combination nowhere show or suggest such a structure as defined in amended claim 10. As already discussed in response to a previous Action, and acknowledged by the Examiner, *Sekine et al.* clearly do not teach or even suggest a chip-on-chip structure, but rather a multi-chip module. Although *Admission* and *Frye et al.* disclose

chip-on-chip structures, neither of them shows or suggests to bond a plurality of semiconductor chips onto a surface of a solid device that includes an undivided wafer having a plurality of semiconductor chip elements formed therein, respectively disposed below the semiconductor chips, such that the semiconductor chips and the semiconductor chip elements are separable into separate respective chip-on-chip structures, by a procedure that includes cutting the wafer along cut lines thereof. A person or ordinary skill in the art therefore would not combine the teachings of either of these secondary references with those of the primary reference, since the secondary references say nothing about and are unrelated to a chip-on-chip structure or its formation on a wafer level. In this regard, the statement in the Action that *Fry et al.* teaches interconnection layouts for chip-on-chip packages and *Admission* teaches chip-on-chip structures for heightening integration density is not responsive to the point noted above that the secondary references say nothing about and are unrelated to a chip-on-chip structure or its formation on a wafer level.

Thus, for the above reasons, it is submitted that a person of ordinary skill in the art is provided with no teachings from which it would be obvious to combine these references to produce the claimed invention. Claim 10 and claim 12 depending therefrom are deemed clearly to be patentable over *Sekine et al.* in view of *Admission* or *Frye et al*, and the rejection accordingly should be withdrawn.

Claim 17 is directed to a method for manufacturing a semiconductor device that terminates with taking out individual pieces of chip-on-chip type semiconductor devices by cutting the semiconductor substrate along predetermined cutting lines. Thus, again, the claimed

invention is directed to the creation of chip-on-chip structures on a wafer level basis, which is followed by cutting the semiconductor substrate along predetermined cutting lines to produce the individual structures. That is, the invention of claim 17 is directed to a method that produces a batch (plurality) of "individual" (separated) "chip-on-chip type semiconductor devices." Thus, the earlier "chip bonding step of bonding a plurality of semiconductor chips face-down onto a surface of a semiconductor substrate with active surfaces of the semiconductor chips opposed to the surface of the semiconductor substrate, in such a manner that the plurality of semiconductor chips and substrate define chip-on-chip structures," is basically the same as or equivalent to the formation of chip-on-chip structures "on a wafer level basis."

No combination of the cited references shows or suggests such a method. Indeed, the very idea of producing individual chip-on-chip structures by forming chips on a substrate, and then cutting them apart, is nowhere shown or suggested. Without this idea, the claimed invention cannot be obtained. Again, the statement in the Action that *Fry et al.* teaches interconnection layouts for chip-on-chip packages and *Admission* teaches chip-on-chip structures for heightening integration density, is not responsive to the point noted above that the secondary references say nothing about, and are unrelated to a chip-on-chip structure or its formation on a level wherein a cutting out step can be performed to take out individual pieces of chip-on-chip type semiconductor devices by cutting a semiconductor substrate along predetermined cutting lines.

Therefore, claim 17, and claims 18-21 depending therefrom are deemed clearly to be patentable over the cited references and the rejection accordingly should be withdrawn.

The Examiner also rejected claims 10 and 12 under 35 USC 103(a) as being unpatentable over *Egawa* in view of *Admission* or *Frye et al.* The rejection respectfully is traversed for reasons similar to those presented against the rejection of these claims over *Sekine et al.* in view of *Admission* or *Frye et al.* That is, *Egawa* clearly, and admittedly by the Examiner, does not teach or even suggest a chip-on-chip, and neither *Admission* nor *Frye et al.* say anything about, and are unrelated to a chip-on-chip structure or its formation on a wafer level, or on a level wherein a cutting-out step can be performed to take out individual pieces of chip-on-chip type semiconductor devices by cutting a semiconductor substrate along predetermined cutting lines. A person or ordinary skill in the art therefore would not combine the teachings of either of these references with those of the primary reference.

Thus, for the above reasons, it is submitted that a person of ordinary skill in the art is provided with no teachings from which it would be obvious to combine these references to produce the claimed invention. Claim 10 and claim 12 depending therefrom therefore are deemed clearly to be patentable over *Egawa* in view of *Admission* or *Frye et al*, and the rejection accordingly should be withdrawn.

The Examiner also rejected claims 3, 4 and 6 under 35 USC 103(a) as being unpatentable over *Sekine et al.* in view of *Fukasawa et al.* and *Ichikawa.* Claim 3 has been amended, and it is submitted that the rejection is inapplicable to amended claim 3 and claims 4 and 6 depending therefrom.

Claim 3 has been amended to clarify that the method of manufacturing a semiconductor device according to the invention includes

(i) forming a back side resin layer on a back side of a semiconductor substrate so that a surface resin layer and the back side resin layer have substantially the same thickness respectively,

(ii) by polishing or grinding the surface resin layer, a surface grinding step that exposes from the surface resin layer projection electrodes that have been formed on a substrate surface,

(iii) bracing the substrate with the back side resin layer until after the surface grinding step, and

(iv) after the surface grinding step, performing a back side grinding step of thinning the semiconductor substrate by

(a) removing the back side resin layer, through polishing or grinding, from the semiconductor substrate provided with the surface resin layer and the back side resin layer, and

(b) further polishing or grinding the back side of the semiconductor substrate from which the back side resin layer has been removed.

An aspect of the invention is that the front grinding step is performed before the back side grinding. The Examiner acknowledges that none of the cited references teaches this feature. He notes that *Fukasawa et al.* discloses formation of resin layers on the front and back surfaces of a semiconductor substrate, that *Ichikawa* discloses formation of a resin layer on the back surface of a semiconductor substrate followed by grinding of a resin layer and then grinding the back surface of the semiconductor substrate, and that *Sekine et al.* disclose

formation of bumps 46 on the front surface of a bare chip device 47 followed by sealing with epoxy resin 48 and then grinding or polishing the front surface until the bumps 46 are exposed. He acknowledges the lack of a specific teaching in the prior art of any particular order of grinding resin layers on opposite sides of a semiconductor substrate. In fact, the prior art does not even disclose one side being subjected to grinding before the other. However, the Examiner has taken a position that the ordering of these steps is not a patentable feature, arguing that "[t]he transposition of process steps where the process are substantially identical or equivalent in terms of function, manner and result has been held to be [sic] not patentably distinguish the processes" citing *Ex parte Rubin* 128 USPQ 440 (Bd. App. 1959)(the Examiner apparently inadvertently misquoted "129" the page number at which the decision may be found in the USPQ).

The Examiner has applied this case on the basis of his opinion that "Applicant's specification merely teaches a preference of order without demonstrating an unexpected result and the instant specification also teaches the sequence of the steps is not critical because the steps can be interchanged." The Examiner also points out that an advantage of the invention which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious," citing *Ex parte Obiaya*, 227 USPQ 58 at 60 (Bd. Pat. App. & Inter. 1985).

Initially, the Applicant would remind the Examiner that before getting to an issue of reversing steps and what flows from following the suggestion of the prior art, which are factors in the cited case law, one first must determine that the reversal of steps and alleged suggestion

to be followed are indeed in the prior art. Applicant would dispute the Examiner's apparent conclusion that they are. In fact, the cited prior art *Sekine et al., Fukasawa et al.* and *Ichikawa* do not disclose any sequence of operation with respect to grinding a front side and back side resin layer. Therefore, Applicant's "reversal" is not a modification of the prior art, because the prior art does not teach any order at all, and the advantage that flows from such "reversal" accordingly does not flow from the prior art. Thus, the case law relied upon is totally inapplicable to the present case.

Moreover, even if an order of grinding were in the prior art, the Applicant still would strenuously disagree with the Examiner's application of law to the facts of this case, for a number of reasons. The fact that the front grinding step can be performed before the back side grinding does not make the ordering noncritical to the invention. We believe that the specification makes clear that the ordering is critical to obtain the benefit discussed on page 30. The fact that according to a broader definition of the invention, the steps could be reversed, does not mean the ordering is not critical to the more narrowly defined invention in which the ordering is specified. Thus, the **ordering is critical** to the **claimed** invention. It also is clear that the function, manner and result are not the same if the steps are reversed because the back side resin layer performs a function during grinding of the front side layer, which clearly it cannot perform if it has already been partially ground away in advance. And of course the result is different in terms of layer uniformity depending on the order of the steps.

The Examiner also takes the position that the specification does not demonstrate that the result of the invention is unexpected. This assertion is deficient in two respects. First of all,

there is no *per se* requirement that a claimed invention attain "an unexpected result" before a conclusion of nonobviousness can be reached. See *Panduit Corp v. Dennison Mfg. Co.*, 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985). Unexpected results is a consideration evidencing unobviousness in response to a rejection based on a combination of prior art teachings to demonstrate that it would not be obvious to combine the references to obtain the claimed invention.

Here, there is no prior art teaching relied upon by the Examiner for the claimed ordering of the grinding steps. Rather, the Examiner asserts that the mere alleged absence of an unexpected result means that reversing steps would be obvious to a person skilled in the art, relying upon MPEP 2144.04 and law cases cited therein. The applicable statements in MPEP 2144.04 are in subsection IV C thereof ("Changes in Sequence of Adding Ingredients"). However, this section of the MPEP is inapplicable to the present invention since claim 3 is not directed to a change in sequence of adding ingredients. Instead, claim 3 recites a specified sequence of operations performed, i.e. grinding steps. Further, *In re Burhans* 154 USPQ 690 (CCPA 1946) (also cited in MPEP 2144.04 IV C) states that selection of any order of performing process steps is *prima facie* obvious in the absence of new and unexpected results. The rejection of the claims of the patent in suit in *In re Burhans* is based on a combination of references that teach each and every one of the claimed steps. And the opinion makes no mention of any result of the ordering of the steps. Further, the cases cited in MPEP 2144.04, subsection IV C, such as *In re Burhans* relate to chemical inventions, different that the present invention. Thus, for this reason as well, the decision is inapplicable to the present application.

Nevertheless, in the present invention, the result is in fact new and unexpected. That the result is unexpected can be inferred from the advantage and the fact that it has not been shown to be known in the prior art. Certainly it is new as there is no prior art of record showing the claimed grinding order (or in fact any order), or of the reduced pre-surface/post-back side grinding warpage. Moreover, if unexpected result is to be considered in the present case, it should not be up to the Applicant to demonstrate that the result is unexpected.

The Examiner states that the order of grinding is not critical because warping may not occur even if the order of grinding is reversed. However, warping is prone to occur if the back side is ground first. What must be kept in mind is that the absence of warpage of the substrate during the front surface grinding step is critical to obtaining electrodes of uniform length, so avoiding warpage is more critical before and during grinding at the front surface than it is afterward. That is, though grinding of the back side first makes uniform polishing or grinding of the back side resin layer more difficult, uniform polishing or grinding of the back side resin layer is less important after the front side has already be ground uniformly.

This may be explained as follows: The Applicant has noted as to the ordering of the surface grinding and the back side grinding, that when the ordering is according to the invention,

1. warpage of the substrate does not occur before the surface grinding step because before the surface grinding step, the surface resin layer and back side resin layer have substantially the same thickness;

2. warpage of the substrate does not occur during the surface grinding step because during the surface grinding step, the substrate may be placed, for example, on a surface of a vacuum chuck and the exposed surface pressed by the surface of the grinding head of a grinder.

3. therefore, because no warpage has occurred before or during the surface grinding step, there can be no interference from warpage with the efforts to obtain projection electrodes of uniform height at the surface.

To the contrary, if the back side grinding step is performed first and the surface grinding step is performed thereafter, then warpage of the substrate is prone to occur during the time following the back side grinding and before the surface grinding step. In this case, at the initial stage of the surface grinding step, this surface may not uniformly contact with the grinding head of a grinder, so that uniform polishing or grinding of the side resin layer may become difficult, and any non-uniformity of such grinding in turn results in non-uniform heights of projection electrodes on the surface of the substrate.

Thus, there is a substantial difference between the results obtain by the method of the invention and that obtained if the references were combined in the manner suggested by the Examiner and the grinding were performed first at the surface. This contrasts with the situation described in *In re Rubin*, where (1) the appellant conceded that the same product is obtained by either the claimed method or where the steps in question are reversed, and (2) moreover, while the claimed ordering of steps is satisfactory, the prior art method was actually *"considered the better of the two methods . . "*. A Board opinion where the prior art method actually is admitted

to be the better one, should hardly be relied upon as authority in an analysis of how dramatic an improvement must be provided for it to be a patentable one.

To emphasize a function of the elements, claim 3 has been amended to make explicit that by grinding the back side last, the substrate is braced with the back side resin layer until after the surface grinding step.

A further point we would reiterate from Applicant's previous office action response, is that choosing to conduct the back side or front side grinding first is not a simple matter of design choice. It must be kept in mind in this regard that a manufacturer seeking to improve on the method of the primary reference, *Sekine et al.*, has first to make many choices that result in several other claimed steps before even getting to the issue of order of grinding, as described, for example, by the Examiner on pages 8-10 of the present office action. It would therefore be a gross oversimplification to say that to obtain the invention, a skilled person need only select between two orders of grinding. Moreover, we would note that while the specification describes two possible orders of grinding as being possible, neither the present specification nor the prior art anywhere states or implies that grinding the front surface first and the back afterward is an alternative known to those skilled in the art.

In view of the above, it is deemed to be clear that claim 3 and claims 4 and 6 depending therefrom clearly are patentable over the cited references. The rejection accordingly should be withdrawn.

Therefore, based on the above, it is submitted that this application is in condition for allowance. Such a Notice, with allowed claims 3, 4, 6, 10, 12 and 17-21, and 26 - 29, earnestly is solicited.

Applicant's counsel acknowledges with thanks the Examiner's courtesy, and helpfulness in airing the issues, during an office conference conducted on February 28, 2005. Should the Examiner feel that a further conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such a conference. Should any additional fee be required, or if no payment is attached, please charge the same to our Deposit Account No. 18-0002 and advise us accordingly.

Respectfully submitted,

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Date

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